COMMUNICATION AND NETWORKING RISER ECR FORM

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ECR# (assigned internally): #011

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Title of the Change: **Main Board AC97 CODEC Disable Circuit**

Specification Title and Version: **CNR Specification, Version 1.0**

Reason for Change:
Not all AC97 CODEC manufacturers hold Bit_CLK and SDATA_IN in a high impedance state while in reset.

Description of Change:
Allow automatic disable of a CODEC residing on the main board by driving the CODEC SDATA_OUT input pin with the logical OR of the controller's SDATA_OUT signal and the CDC_DN_ENAB# signal.

The changes to the CNR Specification will only require that the addition of the following text and figure, after Figure 13 (page 25) in the CNR Specification.

An optional method for disabling the codec on the motherboard is shown (inside dashed box) in Figure ??. This method places the AC '97 codec on the motherboard into the codec's ATE test mode (as defined by the AC '97 Specification). This is accomplished by ORing the SDATA_OUT signal, to the codec, with the CDC_DN_ENAB# signal.

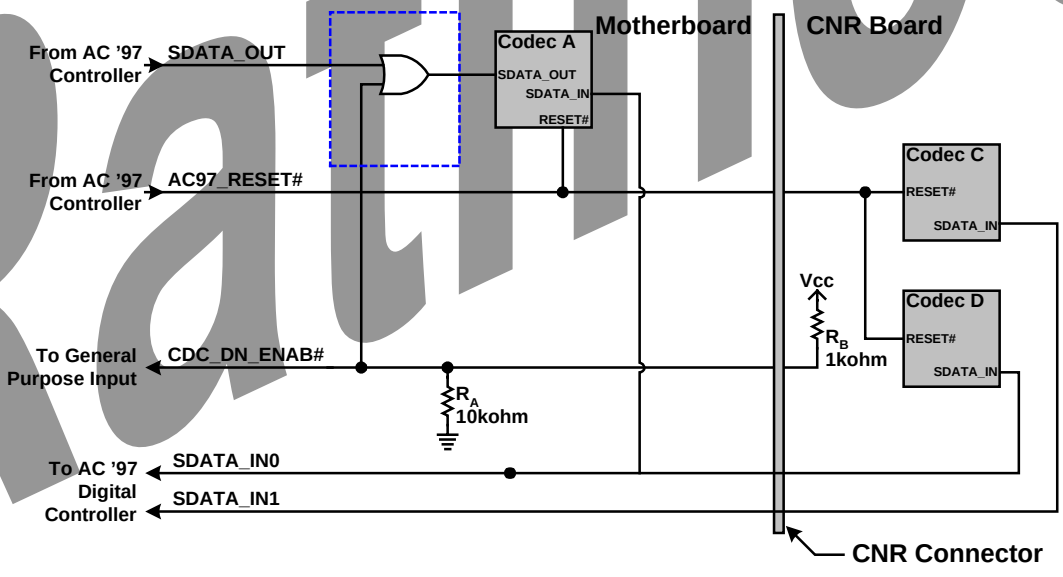

Figure ?? – Optional motherboard codec disable circuit

Note: The motherboard designer must make sure that all AC '97 timing requirements are met when implementing the above codec disable circuit of Figure ??

Ratified